High Temperature Characteristics of 5 kV, 20 A 4H-SiC PiN Rectifiers

Ranbir Singh, Allen R. Hefner*, David Berning*, John W. Palmour
Cree, Inc., 4600 Silicon Dr., Durham NC 27703, USA.
*[1]NIST, Semiconductor Electronics Div., 100 Bureau Dr., Stop 8123, Gaithersburg, MD 20899, USA.
919-313-5540 (ph), 919-313-5696 (fax), ranbir_singh@cree.com

Abstract— **This paper reports the design, fabrication process, and high temperature characteristics of a 4H-SiC rectifier with a 5 kV, 20 A rating. A highly doped p-type epitaxial Anode layer and junction termination extension (JTE) were used in order to get good on-state and stable blocking characteristics. A forward voltage drop of less than 5 V was observed at 500 A/cm^2 in the entire 25 to 225°C temperature range. The reverse recovery characteristics show only a modest 50% increase in the peak reverse recovery current from 25°C to 225°C. Measurements at a forward current density of 150 A/cm^2 show that a four orders of magnitude reduction in Q_{rr} is obtained in 4H-SiC rectifiers as compared to comparably rated Si rectifiers.**

Index Terms— **SiC, PiN, rectifier, reverse recovery.**

I. Introduction

Power devices made with Silicon Carbide (SiC) are expected to show great performance advantages as compared to those made with other semiconductors. This is primarily because 4H-SiC has an order of magnitude higher breakdown electric field (2-4X10^6 V/cm) than Si and GaAs, and an electron mobility only ~20% lower than silicon. A high breakdown electric field allows the design of SiC power devices with thinner and higher doped voltage-blocking layers.

High voltage PiN diodes made using conventional semiconductor materials are restricted to <50 kHz and <120°C, thereby severely limiting the availability of advanced electronic hardware used for energy storage, pulsed power, intelligent machinery and solid state power conditioning. These components require high power density, very high frequency, and high temperature devices like the 4H-SiC PiN rectifier. The first successful attempt in the demonstration of a >5 kV 4H-SiC rectifier was done using a 4H-SiC n$^-$ epitaxial layer with a thickness of 85 μm and a doping of 1-7E14 cm^{-3} [1]. Other demonstrations [2,3] of >3kV 4H-SiC PiN rectifiers show that extremely high switching speeds and an on-state voltage drop comparable to Si PiN diodes are achieved when operated at sufficiently high current densities. The biggest challenges facing the realization of such high voltage rectifiers is the design of the edge termination, and the growth of pure, low defect density epitaxial layers with sufficiently high minority carrier lifetimes. The advent of hot wall epitaxial reactors have enabled the growth of >40 μm 4H-SiC epitaxial layers with good carrier lifetimes. In the recent past, minority carrier lifetimes have been improved to a level that enables the realization of high voltage SiC rectifiers with <4.5 V on-state drop at 100 A/cm^2.

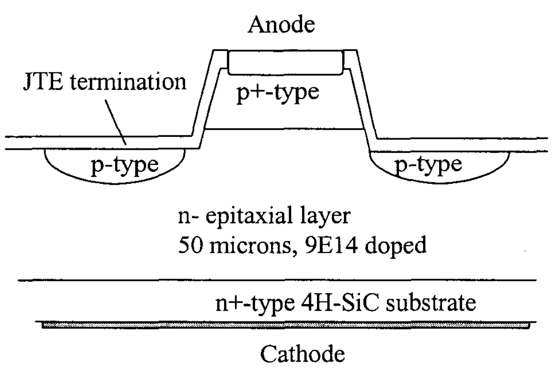

Figure 1: Cross-section of a high voltage 4H-SiC PiN rectifier using a highly doped epitaxially grown Anode layer and etched and implanted JTE structure.

II. Device Design And Fabrication

The cross-section of the 4H-SiC PiN rectifier reported in this paper is shown in Figure 1. These rectifiers were made using a 50 μm thick voltage blocking epitaxial layer with a doping of N_D=9E14 cm^{-3} grown on low micropipe density (<30 μP/cm^2) 4H-SiC n$^+$ substrates. To achieve a high, activated p+ concentration, the Anode region was also epitaxially grown. This enables a high concentration of injected holes into the low doped drift layer during the on-state operation of the rectifier. A high concentration of these minority carriers results in a low on-state voltage drop.

Edge termination design

From a device design standpoint, the biggest challenge in achieving high voltage PiN diodes is the design and implementation of an effective edge termination. Such a technique is expected to make the electric field distribution uniform at the edge of the device, approaching the ideal breakdown voltage capability of the epitaxial layer used. Traditionally, many techniques like guard rings, floating field rings, and trench guard rings [4] have been used. Another promising edge termination design involves implanting the device edge with an optimum p-type charge (for the typically used n-type epitaxial layer) in order to gradually reduce the electric field from the device edge to the outer periphery of the device structure. This technique is called junction termination extension (JTE). The optimally activated JTE charge depends upon the background

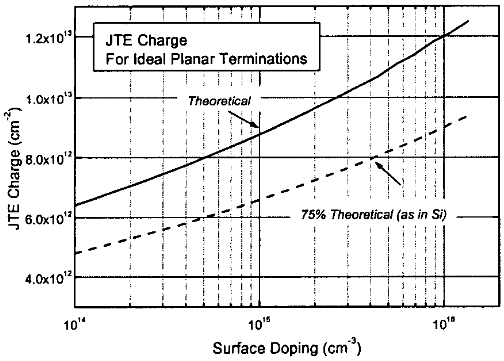

Figure 2: JTE charge vs surface doping of the voltage blocking layer for a SiC device.

doping concentration of the low doped n-type region. A plot showing the ideal total charge per unit area along a vertical cross-section of the implanted JTE region is shown in Figure 2. In silicon, when planar terminations are made using JTE, it has been found that it is safe to implement a JTE charge with about 75% of that predicted by theoretical analysis. This is because JTE charge in excess of the ideal value results in a sharp reduction in the obtained breakdown voltage, while a charge smaller than the optimum does not severely affect the breakdown voltage of the device. The JTE charge corresponding to 75% is also plotted in this graph for silicon carbide.

The fabrication sequence of these rectifiers is as follows: An optimum dose of Boron was implanted at a high temperature after reactive ion etching through the p+ Anode cap layer. A channel stop implant with a high dose of Nitrogen was introduced 100 μm beyond the JTE implant. These implants were annealed at 1625°C followed by a 2 μm LPCVD SiO_2 deposition. Thereafter, backside Ni ohmic metal and Ti Anode metal were deposited. These metals were annealed at a high temperature to form the PiN Anode and backside cathode contacts. These metals were followed by a 2 μm Ti/Pt/Au deposition to reduce the resistance and enable wire bonding.

Rectifiers with active Anode areas of 1mm X 1mm and 2mm X 2mm were fabricated alongside. These devices had rounded edges to minimize concentration of electric field during their reverse bias operation. Devices were diced and wire-bonded for further characterization.

III. Static Characteristics

After their fabrication, these rectifiers were extensively characterized for static and dynamic characteristics. The goal for this study was to obtain a good yield of 4H-SiC rectifiers with a >4.5 kV blocking voltage and a <4 V on-state voltage drop at 100 A/cm^2. This would pave the path for commercial manufacture of such rectifiers. The on-state voltage drop was found to be very uniform across the wafer and was not a yield limiting factor. The robust edge termination design outlined above and its associated processing allowed us

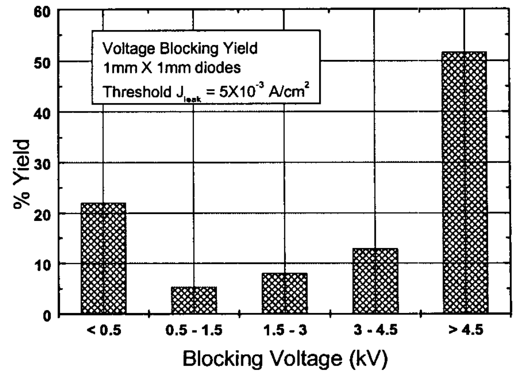

Figure 3: On-wafer yield of >50% was obtained for 1mm^2 rectifiers capable of blocking >4.5 kV for a leakage current density threshold of 5X10^{-3} A/cm^2.

to obtain a yield of >50% for 1 mm^2 rectifiers capable of blocking >4.5 kV when using a low leakage current density threshold of 5X10^{-3} A/cm^2. The percentage distribution of ALL 1 mm^2 devices obtained from the wafer versus blocking voltage ranges is shown in Figure 3. As seen from this figure, 22% of all devices block less than 1500 V, primarily due to materials defects such as micropipes. The reverse bias characteristics of a 2mm X 2mm rectifier are shown in Figure 4. The measured leakage current density was <10^{-3} A/cm^2 at 5 kV and thereafter it increases dramatically at about 5.3 kV. The breakdown characteristics were not catastrophic, with the device surviving after the applied voltage was reduced. High temperature (up to 225°C) measurements were performed only at 2 kV because of equipment limitations. The leakage current increases exponentially with temperature, but was still found to be less than 4x10^{-5} A/cm^2 at 225°C at 2 kV for a 0.04 cm^2 rectifier, as shown in Figure 5. Hence, it can be concluded that this edge termination design is quite robust for devices with a high temperature capability.

The forward I-V characteristics show excellent on-state voltage drop. At a high current density of 1250

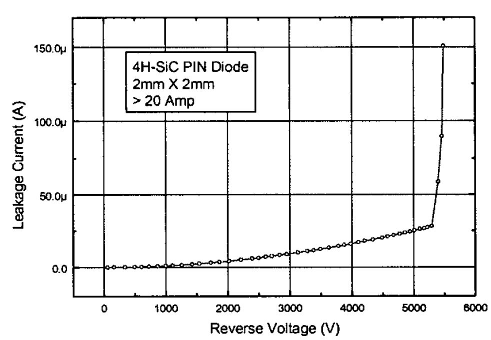

Figure 4: Blocking characteristics of a 5.3 kV rectifier capable of carrying >20 Amperes.

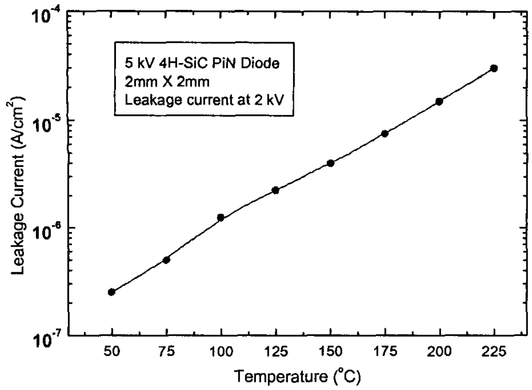

Figure 5: The leakage current density was less than $4x10^{-5}$ A/cm^2 at 225°C at 2 kV for a 0.04 cm^2 rectifier, even after an exponential increase with temperature.

A/cm^2 (50 Amperes on a 2mm X 2mm device), the on-state voltage drop was only 6.9 V, which was significantly affected by the wire bonding resistance. The measured temperature dependence of the on-state characteristics for a 5 kV, 20 A (0.04 cm^2) rated SiC PiN diode is shown in Figure 6. The decrease in on-state voltage with temperature is indicative of the increase in lifetime with temperature for a conductivity modulated device, and a decrease in bandgap of the PN junction. However, at a high temperature of 225°C, a reduction in carrier mobility starts to increase the differential on-resistance across the drift layer. This leads to a cross-over in the I-V characteristics at a high current density of 500 A/cm^2. In the entire 25°C to 225°C range, the on-state voltage drop remains in a somewhat insignificant 0.4 V range, as seen from Figure 6. This shows that SiC PiN diodes are remarkably stable with temperature.

IV. DYNAMIC CHARACTERISTICS

Detailed switching measurements were conducted on some 5 kV blocking 4H-SiC PiN rectifiers. The most

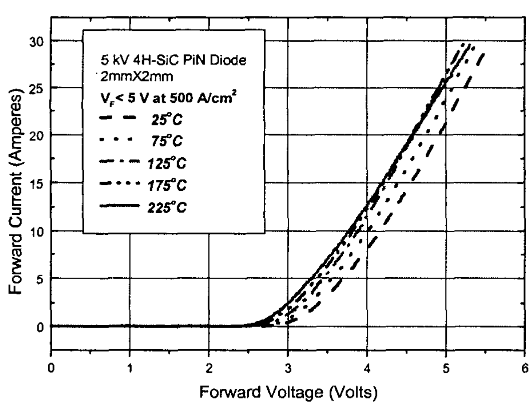

Figure 6: The forward voltage drop decreases slightly with an increase in operating temperature.

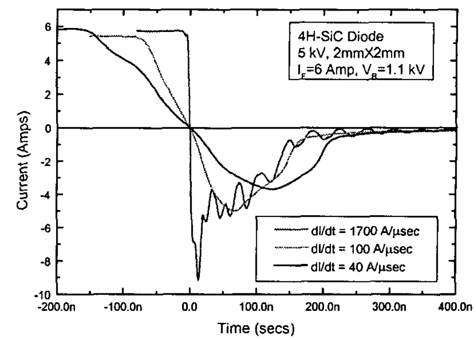

Figure 7: Reverse recovery characteristics show a 2X increase in the peak reverse recovery current when the reverse di/dt was increased from 40 A/µsec to an extremely high 1700 A/µsec.

important dynamic characteristics for a rectifier are its reverse recovery characteristics, and their variation with operating temperature.

Reverse Recovery Measurements

The reverse recovery tests were performed for various values of di/dt. Figure 7 shows the current vs. time waveforms of the 20 A, 5 kV SiC PiN diode for three different reverse di/dt values. At the conventional 40 A/µsec, the peak reverse current was only 65% of the forward current. As the reverse di/dt was increased to 100 A/µsec, and 1700 A/µsec, the peak reverse current to forward current ratio increased to 90% and 150%, respectively. As compared to high voltage Si PiN rectifiers, this is a relatively insignificant change, considering that extremely high reverse di/dt values were used.

High temperature switching measurements

The temperature dependence of the rectifier switching characteristics for a 2mm x 2mm 5 kV device is shown in Figure 8. These measurements are taken at a relatively

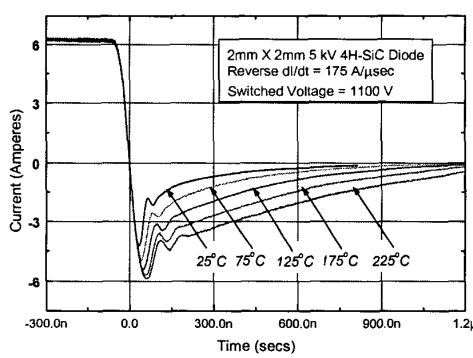

Figure 8: High temperature reverse recovery characteristics show a modest increase in the peak revrse current as the operating temperature is increased from 25°C to 225°C.

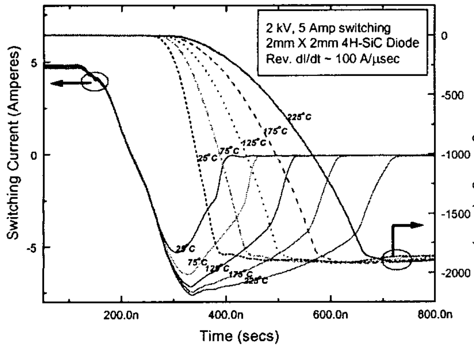

Figure 9: Current and Voltage waveforms of a 5 kV rectifier switched at 25°, 75°, 125°, 175° and 225°C.

high reverse di/dt of 175 A/µsec, when the diode is switching 1100 V at 6.2 Amperes. As seen from this figure, the peak reverse current increases by a modest 50% when the temperature was increased from 25°C to 225°C. The total reverse recovery charge, which is the area under the I-t curve when the rectifier is undergoing reverse recovery, increases by approximately 100%, as the operating temperature is increased from 25°C to 225°C. These rectifiers show fairly stable switching characteristics as the operating temperature was increased from 25°C to 225°C. The turn-off time increases from 0.2 µsec to 0.65 µsec while switching 125 A/cm^2 (5 A) and 2 kV with a reverse dI/dt of 100 A/µsec, as shown in Figure 9. These rectifiers do not show a "snappy" recovery and have substantially smaller noise signatures when compared to 600 V Silicon PiN rectifiers.

V. Discussion

Figure 10 shows that the on-state voltage drop changes from 3.9 V to 3.4 V at 150 A/cm^2 as the operating temperature is increased from 25°C to 225°C. Under the same conditions, the measured reverse recovery charge increases from 0.5X10^{-7} C to 1.3X10^{-7} C. This is a 10^{4}X reduction in Q_{rr} as compared to comparably rated Si rectifiers. It is worthwhile to note that switching behavior dramatically worsens with temperature for Si diodes. Two factors contribute to the dramatically smaller reverse recovery charge (Q_{rr}) in 4H-SiC rectifiers as compared to similarly rated Si rectifiers: (a) the 20-25X thinner voltage blocking layers with 20X higher doping reduce the total volume of excess charge in the drift layer; and (b) the carrier lifetime required for these thinner voltage blocking layers can be >10X smaller than those required for Si devices for a similar mid-region voltage drop. A much smaller carrier lifetime and thinner voltage blocking layer in 4H-SiC results in a very stable on-state voltage drop with temperature. Since switching speed is the primary source of losses in most power conditioning circuits, this improvement is very significant for the realization of next generation, advanced military and utility hardware.

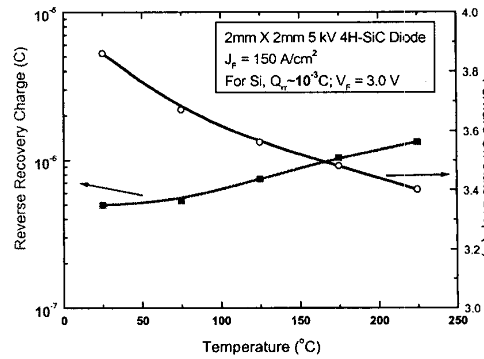

Figure 10: A 10^4 X reduction in switching power losses with similar on-state performance can be expected from 5kV 4H-SiC PiN rectifiers as compared to Si PiN rectifiers with similar ratings.

Acknowledgements

The authors gratefully acknowledge the support of the Defense Advanced Projects Agency's MEGWATT Program under an Office of Naval Research contract, N00014-98-C-0191, monitored by Dr. George Campisi.

References

[1] R. Singh, K. G. Irvine, O. Kordina, J. W. Palmour, M. E. Levinshtein, and S. L. Rumyanetsev, "4H-SiC bipolar PiN diodes with 5.5 kV blocking voltage," *Proc. Device Research Conference, Charlottesville, VA*, June 22-24, 1998, pp. 86-87.

[2] K. Rottner, A. Schöner, M. Frischholz, J.-O. Svedberg, U. Gustafsson, A. Ellison, E. Janzen, and O. Kordina, "Design and implementation of a 3.4 kV ion implanted p-i-n rectifier in 4H SiC," *Abstracts of Intern. Conf. on Silicon Carbide, III-nitrides and Related Materials*, Stockholm, Sweden, Aug. 31-Sept. 5, 1997, pp. 136-137.

[3] H. Mitlehner, P. Friedrichs, D. Peters, R. Schorner, U. Weinert, B. Weis and D. Stephani, "Switching behavior of fast high voltage SiC pn diodes," *Proc. of International Symposium on Semiconductor Power Devices and ICs (ISPSD), Kyoto*, June 3-6, 1998, pp. 127-130.

[4] R. Singh, and J. W. Palmour, "Planar terminations in 4H-SiC Schottky diodes with low leakage and high yields," *Proc. of International Symposium on Semiconductor Power Devices and ICs (ISPSD), Weimar, Germany*, May 26-29, 1997, pp. 157-160.